REMARKS

Claims 1-10 are now pending in the application. The purpose of this Preliminary Amendment is to place the English translation of the application in a more traditional U.S. format, and to amend the claims. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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~~[Document] Specification~~

~~[Title of the Invention]~~ SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

~~[Detailed Description of the Invention]~~

~~[0001]~~

[Field of the Invention]

The present invention relates to a semiconductor device suitable for a MOS transistor, and a method of manufacturing the same.

~~[0002]~~

[Description of the Prior Art]

Conventionally, a method of manufacturing a MOS transistor, which is explained below, is known. Taking an N channel MOS transistor as an example, the structure and the method of manufacturing thereof will be briefly explained with reference to FIG. 13.

~~[0003]~~

A p-well region 302 having a carrier density of $3 \times 10^{16}/cm^3$ is formed on~~in~~ an n-type silicon substrate 301 having a carrier density of $2 \times 10^{15}/cm^3$. Next, ions of boron are implanted as the channel doping ion, and a gate oxide layer 303 having a thickness of 20 nm is formed by a thermal oxidation method. Next, phosphorus doped poly silicon having a thickness of 400 nm is deposited by a CVD (Chemical Vapor Deposition) method. Next, a gate region 304 is formed by a conventional photolithography process and a conventional dry etching process. Next, by performing a phosphorus ion implantation process for an N-channel, a self-aligned LDD region 305 is formed (FIG. 13 (a)).

~~[0004]~~

Next, after forming an~~the~~ oxide layer by a~~the~~ CVD method, a highly anisotropic dry etching process is performed. A highly isotropic oxide layer is formed by using the CVD method, while an oxide layer is left only at both sides of the poly silicon by using the highly anisotropic dry etching method, thus forming sidewall regions 306 (FIG. 13 (b)).

~~[0005]~~

And next, phosphorus is implanted with a dose of about $5 \times 10E^{15}/cm^2$, thus forming source/drain regions 307. Moreover, because the regions contain a high concentration of impurity and exhibit low resistivity,

the regions are also used for electrical wiring, which may couples each element.

[0006]

Finally, a lamp annealing process for activating the implanted impurity is performed, thus forming an N channel MOS transistor (FIG. 13 (c)).

[0007]

Although a process of manufacturing an N channel MOS transistor is described above, this process can also be used to ~~becomes a process of~~ manufacture~~ing~~ a P channel MOS transistor by changing ion sources in an ion implantation process.

[0008]

With the demand for down-sizing of MOS transistors and for increasing the speed of MOS transistors, a salicide (Self-aligned Silicide) technology, which simultaneously silicides the surface of the gate region and the source/drain regions in a self-aligned manner, is commonly used to reduce resistivity in the gate region and the source/drain regions. Using~~With adopting~~ this technology, each electrode surface is covered with a low resistive silicide such as titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$), thus reducing the sheet resistivity thereof.

[0009]

However, when ~~a thermal processing is performed to~~ a Si substrate covered with a Co layer is subjected to thermal processing, Co diffuses into the Si substrate to form a compound of CoSi. In this case, Co easily diffuses deep into the substrate by tracing residual defects of a linear shape, which remain inside the Si substrate. Moreover, Co tends to condense around the defects~~,~~. eConsequently, a phenomenon that ~~Co_2Si~~$CoSi_2$ grows unusually through the defects deeply into the substrate occurs. If the unusually grown ~~Co_2Si~~$CoSi_2$ reaches the vicinity of the P/N junction of the well and the diffusion layer, a junction leakage occurs ~~therefrom~~.

[0010]

In order to solve this problem, ~~in the Patent Document 1,~~ a technique of implanting an impurity into source/drain ~~two~~in separate ~~two~~ times has been used~~is adopted~~. ~~Namely, i~~In this technique, a first impurity implanting process is performed such that a light impurity concentration is deeply implanted~~so as to implant deeply~~ into the source/drain ~~with a light~~

~~impurity concentration~~. Accordingly, the residual defects are reduced by lowering the impurity concentration of the source/drain regions, which in turn~~thus~~ suppresses~~ing~~ the unusual growth of ~~Co_2Si~~$CoSi_2$ as well as~~and~~ the junction leakage caused by the unusual growth.

~~[0011]~~

However, ~~if~~ by simply reducing the impurity concentration of the source/drain regions, the contact resistance with the $CoSi_2$ layer formed thereon increases. As such~~So, in the invention of the Patent Document 1~~, a second impurity implanting process is performed at a shallow~~ly in~~ depth to form~~and with~~ an impurity concentration as high as possible. Namely, a heavily doped layer containing many residual defects is formed underneath the $CoSi_2$ layer. ~~Namely b~~By causing many defects to occur over the whole surface of the heavily doped layer and causing the unusual growth of the ~~Co_2Si~~ $CoSi_2$to occur uniformly over the whole surface of the heavily doped layer and terminate there, a part of the ~~Co_2Si~~ $CoSi_2$ is prevented from growing prominently deep, thereby suppressing the junction leakage more effectively.

~~[0012]~~

In addition, ~~the Patent Document 1 discloses that~~ a second ~~time~~ ion implanting process for forming the heavily doped layer needs to be performed with a dose amount of at least 1 x $10E^{15}/cm^2$, to reduce the unusual growth of ~~each~~ ~~Co_2Si~~ $CoSi_2$.

~~[0013]~~

~~[Patent Document 1]~~

~~Re-publication patent WO 99/16116~~

~~[0014]~~

~~[Problem to be Solved by the Invention]~~

Si becomes amorphous when~~by~~ implanted~~ing~~ with a high impurity concentration. As such~~Then~~, for restoring the amorphized Si and activating the implanted impurity~~, for example~~, a RTA (rapid thermal annealing) is performed at 1020°C, for example. With this annealing, a solid phase epitaxial growth arises to restore the defects. However, the solid phase epitaxial growth exhibits a plane direction that~~o~~ leaves small defects along the plane direction of <111>.

~~[0015]~~

In recent years, an isolation technology using a shallow trench

isolation (hereinafter referred to "STI") method has been adopted. As for the STI, a trench groove is formed in the boundary of elements to embeded SiO_2 in the trench groove, thus isolating the elements.

[0016]

To manufacture a device having high breakdown voltage, a gate region having a relatively thick layer may be formed in a gate oxidization step. Therefore, in such a gate oxidization step, oxidization growth in the trench groove of the STI is also accelerated to cause a strong stress to be retained inside the silicon substrate.

[0017]

Then, a huge dislocation loop originating from a tiny residual defect in the source/drain regions may occur to extend to the bottom edge portion of the trench groove. This huge dislocation loop has a problem of crossing the P/N junction and generating a leakage current.

[0018]SUMMARY OF THE INVENTION

The present invention has been made in view of thein above problems, and, therefore, an object of the invention is to provide a semiconductor device, and a method of manufacturing the same, which can prevent the generation of athe junction leakage by forming a diffusion layer with a concentration as low as possible. Alternatively, the junction leakage can be prevented or by forming the diffusion layer by using a two-step ion implantioning of two times with two different impurity concentrations so as to make the concentration of a heavily doped layer as low as possible and the depth of the heavily doped layer as shallow as possible.

[0019]

[Means to Solve the Problem]

In view of the above objects of the invention, Aa semiconductor device according to the present invention comprises: a semiconductor region, in which an impurity of one conductivity type is doped, a gate insulation layer, formed on the semiconductor region, and a gate electrode, formed on the gate insulation layer. Furthermore, a lightly doped layer is, formed in a region from athe principal surface to a first depth of the semiconductor region, In this manner, which a first impurity of the another conductivity type is implanted with a first dose amount, and a heavily doped layer that, is formed in a region from the principal surface of the semiconductor region

to a second depth, which is shallower than the first dept, in which a second impurity of ~~the~~ another conductivity type is implanted into the semiconductor region with a second dose amount in a range of the first dose amount or more to 1 x 10~~E~~^{15}/cm^2 or less.

~~[0020]~~

According to such a structure, the gate insulation layer is formed on the semiconductor region, in which the impurity of one conductivity type is doped, and the gate electrode is formed on the gate insulation layer. The diffusion layer has the lightly doped layer and the heavily doped layer. The lightly doped layer is formed in the region from a~~the~~ principal surface of the semiconductor substrate to the first depth by implanting the first impurity of the other conductivity type into the semiconductor region with the first dose amount. On the other hand, the heavily doped layer is formed in the region from the principal surface to the second depth, which is shallower than the first depth, by implanting the second impurity of the other conductivity type into the semiconductor region with the second dose amount in a range of the first dose amount or more to 1 x 10~~E~~15/cm^2 or less. Because the heavily doped layer is ion implanted with the second dose amount of 1 x 10~~E~~^{15}/cm^2 or less, the residual defects can be prevented from occurring in the annealing process for activating the diffusion layer. Accordingly, the generation of the huge dislocation loop, which crosses the P/N junction, is suppressed, thereby reducing the occurrence probability of the junction leakage.

~~[0021]~~

Moreover, a semiconductor device according to the present invention comprises: a semiconductor region, in which an impurity of one conductivity type is doped,; a gate insulation layer, formed on the semiconductor region, and; a gate electrode, formed on the gate insulation layer;. Further, a lightly doped layer is, formed in a region from the principal surface to a first depth of the semiconductor region, in which a first impurity of the other conductivity type is implanted into the semiconductor region with a first dose amount;. Also, ~~and~~ a heavily doped layer, formed in the depth direction from the principal surface of the semiconductor region, in which a second impurity of the other conductivity type is implanted into the semiconductor region with a second dose amount so that a peak position of the concentration exists at a second depth position, which is shallower than the

first depth by 0.15 μm or more.

[0022]

According to such a structure, the gate insulation layer is formed on the semiconductor region, in which the impurity of one conductivity type is doped, and the gate electrode is formed on the gate insulation layer. The diffusion layer has the lightly doped layer and the heavily doped layer. The lightly doped layer is formed in the region from the principal surface of the semiconductor region to the first depth by implanting the first impurity of the other conductivity type into the semiconductor region with the first dose amount. On the other hand, the heavily doped layer is formed by implanting the second impurity of the other conductivity type into the semiconductor region with the second dose amount so that the peak position of the concentration exists at the second depth, which is shallower than the first depth by 0.15 μm or more. Because the first depth, namely the P/N junction position, is separated by 0.15 μm or more from the peak position of the concentration of the heavily doped layer, even when the residual defects arise in the heavily doped layer, the ~~occurrence~~ probability of the huge dislocation loop, which crosses the P/N junction, occurring is very low. As such, ~~thereby~~ the junction leakage can be suppressed.

[0023]

Moreover, a semiconductor device according to the present invention comprises: a semiconductor region, in which an impurity of one conductivity type is doped; a gate insulation layer, formed on the semiconductor region, and; a gate electrode, formed on the gate insulation layer. Further, a lightly doped layer, formed in a region from the principal surface to a first depth of the semiconductor region, in which a first impurity of the other conductivity type is implanted into the semiconductor region with a first dose amount. Also, ~~and~~ a heavily doped layer, formed in the depth direction from the principal surface of the semiconductor region, in which a second impurity of the other conductivity type is implanted into the semiconductor region with a second dose amount in a range of the first dose amount or more to 1 x 10^{15}/cm^2 or less so that a peak position of the concentration exists at the second depth position, which is shallower than the first depth by 0.15 μm or more.

[0024]

According to such a structure, the gate insulation layer and the gate

electrode are formed in the semiconductor region. The diffusion layer has the lightly doped layer and the heavily doped layer. The lightly doped layer is formed in the region from the principal surface to the first depth by implanting the first impurity of the other conductivity type with the first dose amount. On the other hand, the heavily doped layer is formed by implanting the second impurity of the other conductivity type with the second dose amount in a range of the first dose amount or more to 1 x $10E^{15}/cm^2$ or less so that the peak position of the concentration exists at the second depth position, which is shallower than the first depth by 0.15 μm or more. Namely, the residual defects in the heavily doped layer are suppressed, and even if the residual defects arise, the distance from the residual defects to the P/N junction is 0.15 μm or more, which is long enough to suppress the generation of the huge dislocation loop, which crosses the P/N junction, to thereby reduce the ~~occurrence~~ probability of the junction leakage occurring ~~can be reduced~~.

~~[0025]~~

Moreover, the one conductivity type is N-type and the other conductivity type is P-type.

~~[0026]~~

According to such a structure, an ~~the~~ N-type transistor having a reduced junction leakage is obtained.

~~[0027]~~

Moreover, the second impurity is arsenic.

~~[0028]~~

According to such a structure, even with the heavily doped layer containing the impurity of arsenic, which is liable to produce a defect by an ion implantation, the generation of the residual defects is suppressed, and the residual defects arise at the position sufficiently distant from the P/N junction, thereby the junction leakage can be sufficiently reduced ~~sufficiently~~.

~~[0029]~~

Moreover, the semiconductor device includes a trench structure, which isolates the semiconductor region.

~~[0030]~~

According to such a structure, the generation of the huge dislocation loop originating from the residual defects of the heavily doped layer to the

edge portion of the trench structure can be suppressed.~~,~~ As such, ~~thereby~~ the junction leakage can be reduced.

~~[0031]~~

Moreover, a method of manufacturing a semiconductor device according to the present invention comprises: forming a semiconductor region by doping an impurity of one conductivity type~~;~~, forming a gate insulation layer on the semiconductor region~~;~~, and forming a gate electrode on the gate insulation layer~~;~~. The method also includes forming a lightly doped layer in a region from the principal surface to a first depth of the semiconductor region by implanting a first impurity of the other conductivity type into the semiconductor region with a first dose amount~~;~~, and forming a heavily doped layer in a region from the principal surface of the semiconductor region to a second depth, which is shallower than the first depth, by implanting a second impurity of the other conductivity type into the semiconductor region with a second dose amount in a range of the first dose amount or more to 1 x 10^{15}/cm^2 or less.

~~[0032]~~

According to such a structure, the gate insulation layer is formed on the semiconductor region, and the gate electrode is formed on the gate insulation layer. The lightly doped layer is formed at first in the diffusion~~storing~~ layer, which has the lightly doped layer and the heavily doped layer. The heavily doped layer is formed in the region from the principal surface to the second depth, which is shallower than the first depth by implanting the second impurity of the other conductivity type into the semiconductor region with a second dose amount in a range of the first dose amount or more to 1 x 10^{15}/cm^2 or less. Because the heavily doped layer is ion-implanted with the second dose amount of 1 x 10^{15}/cm^2 or less, the residual defects can be prevented from arising in the annealing process for activating the diffusion layer. Accordingly, the generation of the huge dislocation loop, which crosses the P/N junction, is suppressed which~~,~~ ~~thereby~~ reduce~~sing~~ the ~~occurrence~~ probability of the junction leakage occurring.

~~[0033]~~

Moreover, a method of manufacturing a semiconductor device according to the present invention comprises: forming a semiconductor region by doping an impurity of one conductivity type~~;~~, forming a gate

insulation layer on the semiconductor region; and forming a gate electrode on the gate insulation layer. The method also includes forming a lightly doped layer in a region from the principal surface to a first depth of the semiconductor region by implanting a first impurity of the other conductivity type into the semiconductor region with a first dose amount, and forming a heavily doped layer in the depth direction from the principal surface of the semiconductor region by implanting a second impurity of the other conductivity type into the semiconductor region with a second dose amount so that a peak position of the concentration exists at a second depth position, which is shallower than the first depth by 0.15 μm or more.

[0034]

According to such a structure, the gate insulation layer is formed on the semiconductor region and the gate electrode is formed on the gate insulation layer. The lightly doped layer is formed at first in the diffusion layer, which has the lightly doped layer and the heavily doped layer. Next, the heavily doped layer is formed by implanting the second impurity of the other conductivity type into the semiconductor region with the second dose amount. In this case, the heavily doped layer is formed so that the peak position of the concentration exists at the second depth, which is shallower than the first depth by 0.15 μm or more. Accordingly, the distance from the residual defects that arise in the heavily doped layer to the P/N junction is sufficiently long, and the occurrence probability of the huge dislocation loop, which crosses the P/N junction, is very low, thereby the junction leakage can be suppressed.

[0035]

Moreover, a method of manufacturing a semiconductor device according to the present invention comprises: forming a semiconductor region by doping an impurity of one conductivity type; forming a gate insulation layer on the semiconductor region; and forming a gate electrode on the gate insulation layer. The method also includes forming a lightly doped layer in a region from the principal surface to a first depth of the semiconductor region by implanting a first impurity of the other conductivity type into the semiconductor region with a first dose amount, and forming a heavily doped layer in the depth direction from the principal surface of the semiconductor region by implanting a second impurity of the other conductivity type with a second dose amount in a range of the first

dose amount or more to 1 x 10E^{15}/cm^2 or less so that the peak position of the concentration exists at a second depth position, which is shallower than the first depth by 0.15 μm or more.

[0036]

According to such a structure, the gate insulation layer is formed on the semiconductor region and the gate electrode is formed on the gate insulation layer. The lightly doped layer is formed at first in the diffusion~~storing~~ layer, which has the lightly doped layer and the heavily doped layer. The heavily doped layer is formed in the semiconductor region by implanting the second impurity of the other conductivity type into the semiconductor region with the second dose amount in a range of the first dose amount or more to 1 x 10E^{15}/cm^2 or less. In this case, the heavily doped layer is formed so that the peak position of the concentration exists at the second depth, which is shallower than the first depth by 0.15 μm or more. Accordingly, the generation of the residual defects in the heavily doped layer is suppressed, and even if the residual defects arise, the distance between the residual defect and the P/N junction is sufficiently long, and the occurrence probability of the huge dislocation loop, which crosses the P/N junction, is very low. As such, ~~thereby~~ the junction leakage can be suppressed.

[0037]

Moreover, a semiconductor device according to the present invention comprises: a semiconductor region, in which an impurity of one conductivity type is doped; a gate insulation layer, formed on the semiconductor region; and a gate electrode, formed on the gate insulation layer. The device also includes ~~and~~ a heavily doped layer, formed by implanting a second impurity of the other conductivity type into the semiconductor region with a second dose amount of 1 x 10E^{15}/cm^2 or less.

[0038]

According to such a structure, the gate insulation layer is formed on the semiconductor region, in which the impurity of one conductivity type is doped, and the gate electrode is formed on the gate insulation layer. The heavily doped layer, which becomes a diffusion layer, is formed in the region to the second depth by implanting the second impurity of the other conductivity type into the semiconductor region with the second dose amount of 1 x 10E^{15}/cm^2 or less. Because the heavily doped layer is ion-

implanted with the second dose amount of 1 x $10E^{15}/cm^2$ or less, the residual defects can be prevented from arising in the annealing process for activating [illegible]. Accordingly, the generation of the huge dislocation loop

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